REMARKS

This is in full and timely response to the Office Action mailed on February 20, 2007.

Because May 20, 2007, three months after the filing date of the Office Action, falls on a Sunday, the period for response is extendable to May 21, 2007, which is the next day that is neither a Saturday, Sunday nor a Federal holiday in the District of Columbia.

Accordingly, the filing of this Amendment is timely.

Claims 1-9 are currently pending in this application, with claims 1, 4, 5, 6, and 9 being independent. *No new matter has been added.*

Reexamination in light of the following remarks is respectfully requested.

Information Disclosure Statement

Appreciation is expressed for the listing of the Shibazaki reference on PTO-Form 892.

Specification objection

Paragraph 3 of the Office Action indicates an objection to the specification.

Please hold this objection in abeyance at this time until the other art rejections have been overcome.

At that stage, an appropriate response may be addressed if still deemed necessary.

Rejection under 35 U.S.C. §112, first paragraph

Paragraph 5 of the Office Action indicates a rejection of claims 1 and 4-6 under 35 U.S.C. §112, first paragraph.

This rejection is traversed at least for the following reasons.

In response to this contention, "the purpose of the 'written description' requirement is broader than to merely explain how to 'make and use'; the applicant must also convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention." *Vas-Cath Inc. v. Mahurkar*, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). See also M.P.E.P §2163.02. "How the specification accomplishes this is not material. *It is not necessary that the application describe the claim limitations exactly*, but only so clearly that persons of ordinary skill in the art will recognize from the disclosure that the [Applicant] invented [the claimed invention]. The primary consideration is factual and depends on the nature of the invention and the amount of knowledge imparted to those skilled in the art by the disclosure." (Citations Omitted, emphasis added). *In re Wertheim*, 262, 191 USPQ 90, 96 (CCPA 1976).

"The applicant does not have to utilize any particular form of disclosure to describe the subject matter claimed." *In re Alton*, 37 USPQ2d 1578, 1581 (Fed. Cir. 1996). "The invention is, for purposes of the 'written description' inquiry, whatever is *now claimed*" (emphasis added). *Vas-Cath Inc. v. Mahurkar*, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991).

Furthermore, an applicant for patent is entitled to select the claim language as long as the meaning is reasonably plain and specific. *Ellipse Corporation v. Ford Motor Company*, 312 F.Supp. 646, 660, 164 USPQ 161, 171 (N.D. Ill. 1969). The plain meaning of claims language is entitled to a strong presumption that it correctly expresses the scope of the claim. *In re Certain Thermometer Sheath Packages*, 205 USPQ 932, 941 (ITC 1979).

"A patentee can be his own lexicographer provided the patentee's definition, to the extent it differs from the conventional definition, is clearly set forth in the specification." *Beachcombers v.*

Wildewood Creative Prods., Inc., 31 USPQ2d 1653, 1656 (Fed. Cir. 1994). "For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims." *General Electric Co. v. Nintendo Co.*, 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

Attached below is Figure 2 of the specification as originally filed.

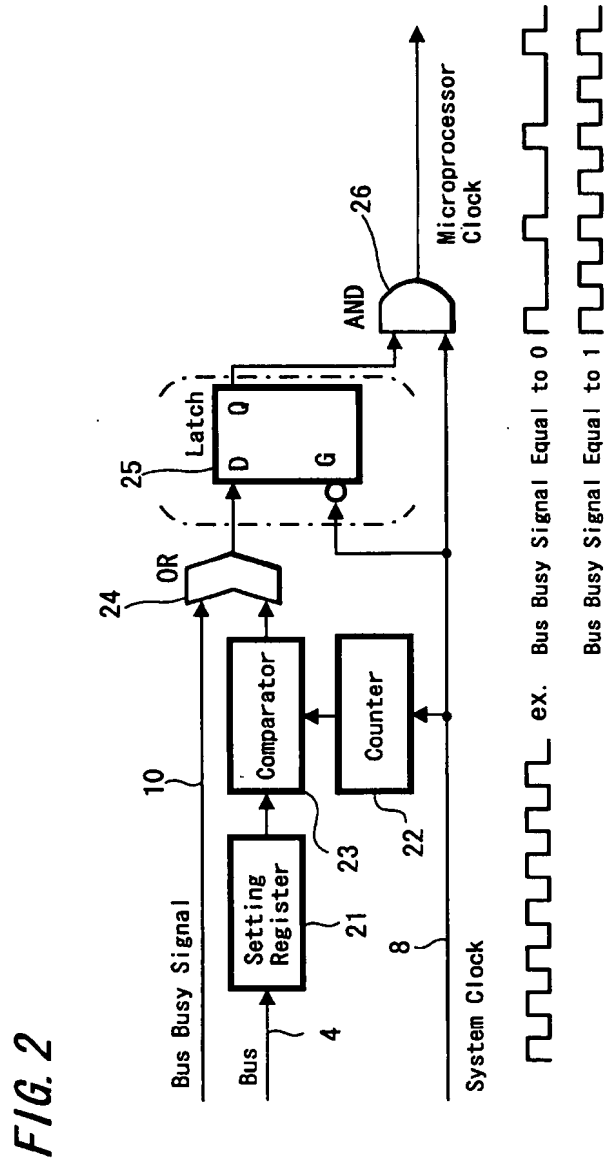

FIG. 2

The following description is provided for illustrative purposes and is not intended t o limit the scope of the invention.

The specification as originally filed beginning at page 9, line 21, provides the following:

> FIG. 2 shows an example of a configuration of the clock control device 2. As shown in the figure, in the case where the bus busy signal 10 from the microprocessor 1 exists, in other words, when the signal state is in "1" state, during the "1" state, the bus busy signal 10 passes through an OR-gate 24 and D-latch 25 unconditionally and acts on an AND-gate 26 as a gate control signal that permits the pass of the system clock 8, as a result, a clock of the same pulse number as the system clock 8 is obtained as the microprocessor clock 9 during a comparatively long period. Hereupon, as a signal for obtaining the system clock 8 as the same pulse number as the microprocessor clock 9, various kinds other than the bus busy signal 10 are conceivable, and in the case where these signals are also considered, these signals may be logically added with the bus busy signal and then are input to an OR-gate 24.

Thus, the applicant was in possession of the invention as of the filing date, and the invention was sufficiently disclosed through illustrative examples and terminology to teach the skilled artisan how to make and how to use the invention. The requirements of 35 U.S.C. §112, first paragraph, have been realized within the above-identified application.

Before repeating the rejection within a subsequent Office Action, section 2163(III)(B) of the M.P.E.P. compels the review of the basis for the written description rejection in view of the record as a whole, including amendments, arguments, and any evidence submitted by applicant.

If the whole record now demonstrates that the written description requirement is satisfied, section 2163(III)(B) of the M.P.E.P. further instructs that the written description rejection *should not be repeated* within the next Office Action.

But if the written description rejection is repeated, section 2163(III)(B) of the M.P.E.P. additionally provides that the Office Action should include a *full response to the Applicant's rebuttal arguments*, and should also include proper treatment of any further showings submitted by applicant in the reply.

Withdrawal of this rejection and allowance of the claims is respectfully requested.

Claim objection

Paragraph 3 of the Office Action indicates an objection to the claims 2 and 7.

Please hold this objection in abeyance at this time until the other art rejections have been overcome. At that stage, an appropriate response may be addressed if still deemed necessary.

Rejections under 35 U.S.C. §102 and 35 U.S.C. §103

Paragraph 8 of the Office Action indicates a rejection of claims 1, 3-6, and 8 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,898,879 to Kim.

Paragraph 13 of the Office Action indicates a rejection of claims 2, 7, and 9 under 35 U.S.C. §102 as allegedly being unpatentable over Kim in view of Tanenbaum, *Structured Computer Organization*, pp. 10-12, 1984 (Tanenbaum).

At least for the following reasons, if the allowance of the claims is not forthcoming at the very least and a new ground of rejection made, then a ***new non-final Office Action*** is respectfully requested.

These rejections are traversed at least for the following reasons.

Claims 1-8 - Claims 2-3 are dependent upon claim 1. Claim 1 is drawn to a clock control device which controls the number of pulses of an operation clock to a microprocessor at least based on whether or not there is a bus busy signal indicating a bus busy state from said microprocessor, comprising:

> clock control means which supplies the microprocessor with a system clock while the bus busy signal is existing and which supplies the microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing, respectively as an operation clock.

Claim 4 is drawn to a microprocessor comprising a clock control device, wherein the clock control device includes, clock control means which supplies a microprocessor with a system clock while a bus busy signal is existing and which supplies said microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing, respectively as an operation clock.

Claim 5 is drawn to an electronic apparatus comprising as control processing means a microprocessor having a clock control device, wherein said clock control device includes clock control means which supplies a microprocessor with a system clock while a bus busy signal is existing and which supplies said microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing, respectively as an operation clock.

Claims 7-8 are dependent upon claim 6. Claim 6 is drawn to a clock control method in which the number of pulses of an operation clock to a microprocessor is controlled at a source supplying the operation clock at least based on whether or not there is a bus busy signal indicating a bus busy state from said microprocessor, comprising the steps of:

> supplying the microprocessor with an operation clock of the same pulse number as a system clock while the bus busy signal is existing; and

supplying the microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing.

Kim - Kim arguably teaches that, as illustrated in Figure 2, a power consumption reducing apparatus in a bus system, in accordance with a preferred embodiment of the invention, comprises a *CPU 1*, a *generic bus master 3* which asks to use the bus (not shown), a *bus controller 2* which prioritizes bus use and which sends a clock control signal to lower or stop the frequency of a clock signal supplied to the CPU, and a *clock generator 4* which outputs a variable frequency clock signal (Kim at column 2, lines 31-38).

As an initial matter, Kim provides that a *bus master 3* other than the DMA controller and the refresh controller requests the *bus controller 2* for use of the bus with one of the *bus-use requesting signals DRQ0 to DRQ7* (Kim at column 2, lines 44-47).

Once a *signal requesting use of the bus* is received from the bus master 3 (other than the CPU 1), the bus controller 2 sends a *holding signal HOLD to CPU 1* requesting separation of the data or address bus from CPU 1 (step S130) (Kim at column 2, lines 48-53).

The bus controller 2 then senses if a *response signal HLDA*, in response to the signal HOLD, is *output from CPU 1* (Kim at column 2, lines 53-56).

Hold signal HOLD stops usage of the bus (step S140) (Kim at column 2, line 56).

In addition, the *bus controller 2*, after sending the bus-using signal DACK to the bus master 3, *sends a clock controlling signal to the clock generator 4* which ***lowers*** the frequency of clock signal supplied to CPU 1 below a predetermined threshold or transfers the clock generator 4 into a 0 Hz stop clock state (step S160) (Kim at column 2, line 63 to column 3, line 1).

The specification for the present invention provides for a *bus busy signal 10 (automatically generated by hardware) from the microprocessor 1 indicating that the microprocessor-bus 4 is actually in busy state* (Specification at page 9, lines 15-17).

In this regard, Kim ***fails*** to disclose, teach, or suggest that *the clock generator 4 supplies the CPU 1 with* ***a system clock*** *while the bus busy signal is existing*.

Instead, Kim provides that the *bus controller 2 sends a clock controlling signal to the clock generator 4* which ***lowers*** *the frequency of clock signal supplied to CPU 1* (Kim at column 2, line 63 to column 3, line 1).

Moreover, Kim ***fails*** to disclose, teach, or suggest that *the clock generator 4 supplies the CPU 1* with a clock having random gap of a *reduced number of pulses of the system clock* while the *bus busy signal is* ***not*** *existing*.

Instead, Kim provides that, if the bus master 3 is finished, the bus controller 2 sends a clock controlling signal to the *clock generator 4 to* ***restore the clock frequency*** *supplied to the CPU 1* to its former state (step S200) (Kim at column 3, lines 13-16).

Tanenbaum - Tanenbaum fails to account for the features shown to be deficient from within Kim.

Claim 9 - Claim 9 is drawn to a clock control program which controls the number of pulses of an operation clock to a microprocessor at a source supplying the operation clock in accordance with a pulse number control data based on an interrupt signal supplied to the microprocessor from the outside, executing the processing that includes:

> an interrupt factor distinction step of distinguishing an interrupt factor each time when the interrupt signal supplied from the outside; and
>
> a pulse-number-control-data transfer setting step of setting pulse number control data that is set in advance corresponding to the interrupt factor distinguished at the interrupt factor distinction step by transferring to a source supplying the operation clock by a program as microprocessor-clock-pulse-number control data.

Kim - Kim fails to disclose, teach or suggest the presence of microprocessor-clock-pulse-number control data.

Tanenbaum - Tanenbaum fails to account for the features shown to be deficient from within Kim.

Withdrawal of these rejections and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

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Respectfully submitted,

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